



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Nikhil Vishwanath Kelkar

Attorney Docket No.: NSC1P300/P05882

Application No.: 10/824,903

Examiner: Shankle, A.

Filed: April 14, 2004

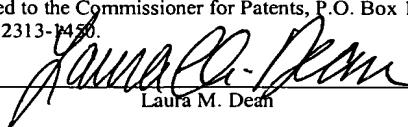
Group: 2891

Title: WAFER LEVEL PACKAGE DESIGN
THAT FACILITATES TRIMMING AND
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Confirmation No: 7593

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the U.S. Postal Service with sufficient postage as first-class mail on July 12, 2006 in an envelope addressed to the Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450.

Signed: 

Laura M. Dean

**INFORMATION DISCLOSURE STATEMENT
BEFORE FINAL ACTION OR NOTICE OF ALLOWANCE
(37 CFR §§ 1.56 AND 1.97(c))**

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

The references listed in the attached PTO Form 1449, a copy of which is attached, may be material to examination of the above-identified patent application. Applicants submit this reference in compliance with their duty of disclosure pursuant to 37 CFR §§1.56 and 1.97. The Examiner is requested to make this citation of official record in this application.

This Information Disclosure Statement is not to be construed as a representation that a search has been made, that additional information material to the examination of this application does not exist, or that this reference indeed constitutes prior art.

This Information Disclosure Statement is being filed after the mailing date of the first Office Action on the merits, or after three months of the filing date of this application, whichever event occurred last, but it is believed before the mailing date of either: (i) a final action under §1.113 or (ii) a notice of allowance under §1.311, whichever occurs first.

Accompanying this Information Disclosure Statement is

a statement as specified in 37 CFR 1.97(e); or
 the fee set forth in 37 CFR 1.17(p).

If fees are due, enclosed is our Check No. 30646 for \$180.00 in payment of the Information Disclosure Statement Fee. If it is determined that any additional fees are due, the Commissioner is hereby authorized to charge such fees to Deposit Account 500388 (Order No. NSC1P300).

Respectfully submitted,
BEYER WEAVER & THOMAS, LLP


Steve D Beyer
Registration No. 31, 234

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Form 1449 (Modified)
**Information Disclosure
Statement By Applicant**

(Use Several Sheets if Necessary)

 Atty Docket No.
NSC1P300/P05882
Applicant:
Kelkar
Filing Date
04/14/2004

 Application No.:
10/824,903
Group
2891

U.S. Patent Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
	A1	2005-0516331	07/21/05	Akram			03/10/05
	A2	2003-0218258	11/27/03	Charles et al.			05/20/03
	A3	2005-0212142	09/29/05	Miyazaki et al.			04/28/05
	A4	2003-0193096	10/16/03	Tao et al.			01/28/03
	A5	2002-0171152	11/21/02	Miyazaki			05/20/02
	A6	2003-0169064	09/11/03	Pirkle et al.			01/15/03
	A7	2003-0129789	07/10/03	Smith et al.			01/29/03
	A8	2003-0127502	07/10/03	Alvarez			12/10/02
	A9	2002-0109228	08/15/02	Buchwalter et al.			02/13/01
	A10	2003-0099767	05/29/03	Fang			12/24/02
	A11	2003-0087475	05/08/03	Sterrett et al.			11/08/01
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	A13	2002-0031868	03/14/02	Capote			09/07/01
	A14	2002-0014703	02/07/02	Capote et al.			08/20/01
	A15	2003-0013233	01/16/03	Shibata			07/11/02
	A16	2002-0003299	01/10/02	Nakamura et al.			03/11/98
	A17	2004-0002181	01/01/04	Scheifers et al.			04/02/03
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	A21	5,329,423	07/12/94	Scholz			04/13/93
	A22	5,736,456	04/07/98	Akram			07/17/96
	A23	5,767,010	06/16/98	Mis, et al.			11/05/96
	A24	5,773,359	06/30/98	Mitchell, et al.			12/26/95
	A25	5,937,320	08/10/95	Andricacos, et al.			04/08/98
	A26	5,977,632	11/02/99	Beddingfield			02/02/98
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	A29	5,214,308	05/25/93	Nishiguchi et al.			01/23/91
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	A33	5,376,403	12/27/97	Capote et al.			10/01/91
Examiner				Date Considered			

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Form 1449 (Modified)				Atty Docket No. NSC1P300/P05882	Application No.: 10/824,903		
Information Disclosure Statement By Applicant				Applicant: Kelkar			
(Use Several Sheets if Necessary)				Filing Date 04/14/2004	Group 2891		

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	A35	5,500,534	03/19/96	Robinson et al.			03/31/94
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	A37	5,668,059	09/16/97	Christie et al.			07/12/96
	A38	5,698,894	12/16/97	Bryant et al.			10/28/96
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	A45	5,895,976	04/20/99	Morrell et al.			06/03/96
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	A54	6,100,114	08/08/00	Milkovich et al.			08/10/98
	A55	6,121,689	09/19/00	Capote et al.			07/21/98
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Examiner				Date Considered			

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Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
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	A69	6,358,627	03/19/02	Benenati et al.			01/23/0
	A70	6,372,547	04/16/02	Nakamura et al.			03/11/9
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Examiner	Date Considered
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		Applicant: Kelkar	
		Filing Date 04/14/2004	Group 2891

Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
	C1	Kulicke & Soffa, Flip Chip Division, Polymer Collar™ Wafer Level Package; “Achieve Maximum Reliability for Wafer Level Packages!”, December 7, 2001, www.kns.com
	C2	Kulicke & Soffa, Flip Chip Division, Polymer Collar™ Wafer Level Package, “See the Polymer Collar™ WLP Difference!”, December 7, 2001, www.kns.com .
	C3	Lau et al., “Chip Scale Package: Design, Materials, Process, Reliability, and Applications,” February 28, 1999, McGraw-Hill Professional Publishing; Chapter 1, pages 1-41.
	C4	Rao R. Tummala, “Fundamentals of Microsystem Packaging,” May 8, 2001, McGraw-Hill Professional Publishing; Chapters 2, 10 and 17.
	C5	“Polymer Collar WLP™, Wafer Level Package Family”, © 2002, downloaded from www.kns.com/prodserv/PDFS/FCD/polymer_collar.pdf , 2 pages.
	C6	“Presenting Polymer Collar WLP™ – A New Wafer Level Package for Improved Solder Joint Reliability”, © 2002, downloaded from www.kns.com/prodserv/flipchip/pdf/PC_ad.pdf , 1 page.
	C7	Barrett et al., Kulicke & Soffa, “Polymer Collar WLP™ – A New Wafer Level Package for Improved Solder Joint Reliability”, © 2002, downloaded from www.kns.com/resources/articles/PolymerCollar.pdf , 9 pages.
	C8	Bogatin, Eric, “All Dressed Up and Nowhere to Go”; Semiconductor International, May 1, 2002, downloaded December 23, 2003, from www.reed-electronics.com/semiconductor/index.asp?layout=article&articleid=CA213812@rid=0&rme=0&cfid=1 , 2 pages.
	C9	Nguyen et al., “Effect of Underfill Fillet Configuration on Flip Chip Package Reliability”, SEMI® Technology Symposium: International Electronics Manufacturing Technology (IEMT) Symposium, SEMICON® West 2002.
Examiner		Date Considered

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Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
	C10	U.S. Patent Application 10/080,913, filed February 21, 2002.
	C11	U.S. Patent Application 10/224,291, filed August 19, 2002.
	C12	U.S. Patent Application 10/707,208, filed November 26, 2003.
Examiner		Date Considered

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